



UNITED STATES DEPARTMENT OF COMMERCE

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| 07/458,507 | 12/28/89 | HORI | R 50120699VC1 |

EXAMINER

BAKER, S

| ART UNIT | PAPER NUMBER |
|----------|--------------|
| 236 | A |

DATE MAILED: 07/27/90

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS This application has been examined Responsive to communication filed on 12/28/90 This action is made final.A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. Notice of References Cited by Examiner, PTO-892.
2. Notice re Patent Drawing, PTO-948.
3. Notice of Art Cited by Applicant, PTO-1449.
4. Notice of Informal Patent Application, Form PTO-152
5. Information on How to Effect Drawing Changes, PTO-1474.
6. _____

Part II SUMMARY OF ACTION

1. Claims 7-19 are pending in the application.

Of the above, claims _____ are withdrawn from consideration.

2. Claims 1-6 have been cancelled.3. Claims _____ are allowed.4. Claims 7-19 are rejected.5. Claims _____ are objected to.6. Claims _____ are subject to restriction or election requirement.7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.8. Formal drawings are required in response to this Office action.9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable; not acceptable (see explanation or Notice re Patent Drawing, PTO-948).10. The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been approved by the examiner; disapproved by the examiner (see explanation).11. The proposed drawing correction, filed _____, has been approved; disapproved (see explanation).12. Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. 140,628; filed on 1/4/88.13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.14. Other

EXAMINER'S ACTION

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1. Claims 7-19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 9 and 14 of claim 7, and in lines 3 and 7 of claim 16, "output" should apparently read as "internal supply". In the last line of claim 13, the relationship of the "and" clause to the rest of the claim is indefinite, however it is assumed to modify the phrase "by controlling". Regarding claims 8 and 14, it is not clear how a "stress" voltage condition differs from any other voltage condition.

2. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

3. Claims 7-19 are rejected under 35 U.S.C. § 103 as being unpatentable over Suzuki.

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Regarding claims 7 and 9-12, first circuits comprise R2, ZD1 and the collector-emitter path through Tr2, second circuits comprise R3, R4, and the base-emitter path through Tr2. An internal supply voltage Eo is provided at the emitter of Tr1. On the shoulder at Ei' of the curve shown in Fig. 3 there is a small portion for which the change in Eo is approximately equal to the change in Ei. Between Ei' and Ei'' can be considered a "normal operating range" where there is a negligible increase in Eo. Above Ei'' can be considered an "aging range" where the slope of Eo is greater than it is between Ei' and Ei".

Regarding claim 13, load circuits comprise Tr2, R2, R3, R4, and ZD1. The internal supply voltage Eo controls the voltage across the load circuits, and also controls a signal on the collector of Tr2 for controlling the voltage limiter.

Suzuki does not disclose the regulator to be on a chip. It would have been obvious to a person having ordinary skill in the art to provide the regulator disclosed by Suzuki on a chip because it would reduce the size and cost, and because chips with regulators were well known at the time the invention was made.

Regarding claims 8 and 14-19, Suzuki does not disclose more than one load transistor, and therefor does not disclose equal "stress voltage conditions" for load transistors. It would have been obvious to a person having ordinary skill in the art to place additional load circuitry on a chip with the regulator

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disclosed by Suzuki because the regulator is intended to drive additional circuitry, and because devices with on-chip regulators were well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art to design a load circuit for the regulator disclosed by Suzuki so that no transistor is significantly more stressed than another under ordinary operating conditions, because eliminating weak links is a well known design goal.

4. The disclosure is objected to because of the following informalities: references to JA 56-168698 should cite the corresponding U.S. Patent instead. Appropriate correction is required.

5. The drawings are objected to because Figs. 13A and 14A should be labelled as prior art. Correction is required. Applicant is required to submit a proposed drawing correction in response to this Office action. However, correction of the noted defect can be deferred until the application is allowed by the examiner.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lewis discloses an IC biasing circuit. Buchsbaum describes an LM7805 regulator chip and an LM903 measurement chip with a built-in regulator circuit.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen

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Baker whose telephone number is (703) 557-4178.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 557-2878.

SMB
July 21, 1990



STEPHEN M. BAKER